



Amendment Under 3, C.F.R. § 1.111
U.S. Application No. 10/648,276

AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

Claims 1.-27. (canceled).

28. (currently amended): A chip manufacturing method, said method comprising:
~~forming a plurality of elements on a wafer; and~~
arranging and forming a said plurality of elements in two or more ~~two~~ lines on a said wafer;
separating said lines with straight cutting paths;
conducting an optical characteristic test with respect to each element;
cutting out a plurality of chips with curved cutting paths, each chip including one of the elements from said wafer;
wherein
each element includes a substantially arcuate shape;
each chip includes a concave boundary line and a convex boundary line that substantially follow an outline of said one of the elements, and
the concave boundary line of one chip of said plurality of chips is shaped as a common line with the convex boundary line of another chip of said plurality of chips that adjoined said one chip on said wafer.

29. (original): The chip manufacturing method as claimed in claim 28, wherein said chips are cut from said wafer using laser beam.

30. (original): The chip manufacturing method as claimed in claim 28, wherein said chips are cut from said wafer using an ultrasonic vibration tool.

31. (original): The chip manufacturing method as claimed in claim 28, wherein said chips are cut from said wafer using hydraulic pressure.

32. (original): The chip manufacturing method as claimed in claim 28, wherein dicing is used to cut the straight-line portions of the contours of said elements.

33. (original): The chip manufacturing method as claimed in claim 28, further comprising mounting a plate on at least a portion of said chip.

34. (currently amended): A chip manufacturing method, said method comprising:
~~forming a plurality of elements on a wafer;~~
arranging and forming ~~asaid~~ plurality of elements in two or more lines on ~~said~~ a wafer;
separating said lines with straight cutting paths;
conducting an optical characteristic test with respect to each element;

cutting out a plurality of first chips with curved cutting paths, each first chip including one of said elements;

cutting out a second chip having a contour that is substantially similar to the contour of said first chip; and

bonding one of said first chips to said second chip;

wherein

each element includes a substantially arcuate shape,

each of said first chips includes a concave boundary line and a convex boundary line that substantially follow an outline of said one of the elements, and

~~wherein~~ the concave boundary line of said one first chip of said first chips is shaped as a common line with the same as the convex boundary line of another chip of said first chips that adjoined said one first chip on said wafer.

35. (original): The chip manufacturing method as claimed in claim 34, wherein said first chip and said second chip are bonded together using an adhesive.

36. (original): The chip manufacturing method as claimed in claim 34, wherein:

said first chip is cut from a first wafer; and

said second chip is cut from a second wafer.